

Regarding the rejection of Claim 8 under 35 U.S.C. § 112, second paragraph, Applicant respectfully submits Figure 7 shows a first surface of a first lead frame 2a corresponding to an upper face of region 3, a second surface corresponding to a lower face of region 3, and a third surface corresponding to a lower face of region 4 of the first lead frame 2a. Further, Claim 8 recites that the third surface is on the same side as the second surface (both facing block 5) and the third surface is closer in a vertical direction to the semiconductor element 1 than the second surface. Therefore, Applicant respectfully submits Claim 8 is definite within the meaning of 35 U.S.C. § 112, second paragraph. Accordingly, it is respectfully requested this rejection be withdrawn.

Claims 1-6 were rejected under 35 U.S.C. § 103(a) as unpatentable over Noda et al in view of Ueno et al. This rejection is respectfully traversed.

Claim 1 is directed to a semiconductor device having a semiconductor element, a lead frame, a metal block, an insulation layer and a bonding material. The metal block improves the heat dissipation characteristic of the whole semiconductor device because of the heat diffusion effect of the metal block.¹

In a non-limiting example, Figure 1 shows the semiconductor element 1, the lead frame 2a, the metal block 5, the insulation layer 7 and the bonding material 10.

Furthermore, a problem that is difficult to increase an area over which heat generated from the power element passes through to the insulation layer was identified in the specification at page 4, lines 10-12, and solved in Claim 1.

On the other hand, Noda et al disclose at column 9, line 63 to column 10, line 6, a device that improves heat dissipation characteristics of the whole device by using materials having higher thermal conductivity than a molding resin placed between a power device 101

¹Specification, page 12, line 10 to page 13, line 5.

and a heat sink 104, and thus the heat diffusion effect of the circuit pattern layer 106 is not expected.

In addition, Ueno et al show in Figure 2 a heating element 1 having a radiator 41 with a protrusion portion 5 placed under a semiconductor device 1. However, Ueno et al do not teach or suggest the radiator 41 used as a circuit pattern.

The radiator 41 in Ueno et al diffuses heat generated from the heating element 1, but because there is no suggestion or motivation to increase a thickness of the circuit pattern layer 106 in Noda et al as the radiator 41 in Ueno et al, Applicant respectfully submits that the teachings of Noda et al and Ueno et al are combined in the outstanding Office Action based on hindsight. Moreover, neither Noda et al nor Ueno et al recognize the problem solved by Claim 1, that it is difficult to increase an area over which heat generated from the power element passes through to the insulation layer.

Further, because the circuit pattern layer 106 in Noda et al functions as the circuit pattern, its shape, in general, is not simple. Therefore, like the lead frame, the circuit pattern layer 106 in Noda et al, in general, is not permitted to increase the thickness thereof in terms of processing problems.

Accordingly, Applicant respectfully submits Claim 1 and each of the claims depending therefrom patentably distinguish over Noda et al and Ueno et al.

Claims 7-8 were rejected under 35 U.S.C. § 103(a) as unpatentable over Noda et al in view of Ueno et al and Applicant's Figure 8. This rejection is respectfully traversed.

The outstanding Office Action recognizes Noda et al and Ueno et al do not show a first surface of the metal block being closer in a vertical direction to a lead frame than a second surface of the metal block and an insulation space between a circuit pattern layer and

a third surface of the lead frame, and relies on Applicant's Figure 8 for teaching these features.²

However, as discussed above, there is no teaching or suggestion in the applied art to increase the thickness of the circuit pattern layer 106 in Noda et al to the thickness of the radiator 41 in Ueno et al. Furthermore, there is no teaching or suggestion to use the metal block 5 as the circuit pattern in Applicant's Figure 8.

Therefore, Noda et al, Ueno et al and Applicant's Figure 8 do not teach or suggest increasing the thickness of the circuit pattern layer 106 to the thickness of the metal block 5. Consequently, even if Applicant's Figure 8 discloses the first surface of the metal block is closer to the lead frame than the second surface of the metal block, Applicant respectfully submits Claim 7 patentably distinguishes over Noda et al in view of Ueno et al and Applicant's Figure 8.

Regarding Claim 8, the outstanding Office Action states Applicant's Figure 8 discloses the semiconductor device in which the third surface of the lead frame is closer to the semiconductor element than the second surface of the lead frame to define an insulation space between the non bonding surface of the metal block and the third surface of the lead frame.

However, as discussed in the Amendment filed July 9, 2002, in contrast to the present invention, Applicant's Figure 8 does not comprise two surfaces that are on a same side and one surface closer to the semiconductor element than the other surface. Furthermore, neither Noda et al nor Ueno et al teach or suggest modifying the surface of the lead frame similar to the present invention.

²Outstanding Office Action, page 5, first paragraph.

Therefore, even if the device of Noda et al is modified based on Ueno et al and Applicant's Figure 8, Applicant respectfully submits the applied art does not achieve the semiconductor device of Claim 8.

Accordingly, Claims 7 and 8 patentably distinguish over the applied art.

Consequently, in light of the above discussion, the present application is believed to be in condition for allowance, and an early and favorable action to that effect is respectfully requested.

Respectfully submitted,

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